

MICROELECTRONIC PACKAGE ARRAY

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MICROELECTRONIC PACKAGE ARRAY**Related Applications**

[0001] This application is a continuation in part of United States Patent Application No. 10/610,854, filed on June 30, 2003.

Field of the Invention

[0002] The present invention relates to microelectronic packaging, and more particularly to increasing package stiffness to enable stacking of multiple microelectronic packages without unnecessarily increasing substrate thickness.

Background

[0003] Trends in microelectronic devices are toward increasing miniaturization, circuit density, operating speeds and switching rates. These trends directly impact the complexity associated with the design and manufacture of microelectronic packages, which may include dice, carrier substrates and the like, as well as computing devices in general. Examples of computing devices include, but are not limited to servers, personal computers and "special" purpose computing devices. Personal computers may have form factors, such as desktop, laptop, tablet, and the like. "Special" purpose computing devices may include set top boxes, personal digital assistants, wireless phones, and the like.

[0004] In particular, attention has increasingly shifted to microelectronic packaging as a way to help meet the demands for enhanced system performance. As demand increases, it has become necessary to use multiple dice and or microelectronic packages that work in conjunction with one another. When using multiple dice or

microelectronic packages, however, it becomes critical to position the dice close together since excessive signal transmission distance may deteriorate signal integrity and propagation times. The use of conventional single-die microelectronic packages, however, is not commensurate with the need to shorten signal transmission distance because they typically have an area (or footprint) many times larger than the area of the die. This not only increases transmission distances, but it also decreases packaging density.

[0005] One solution to create higher density packaging, reduce area requirements and shorten signal transmission distances has been to vertically stack microelectronic packages, such as ball grid arrays (BGA) and chip scale packages (CSP), in an array. Although these stacked microelectronic packages provide certain advantages, further size reduction and performance enhancement has been difficult to obtain due to the physical dimension, design and manufacturing constraints of the individual microelectronic packages and the interconnection to the other microelectronic packages in the array.

[0006] A number of problems exist with stacking microelectronic packages. One problem, for example, is that carrier substrates may warp or flex during manufacturing or under certain operating conditions due to factors such as heat, pressure and weight. Flexing and sag are undesirable because it can result in open connections and reduce solder ball co-planarity, which makes it more difficult to couple microelectronic packages together, electrically and mechanically. These problems can result in microelectronic package failure or significantly reduce effectiveness and performance.

Brief Description of the Drawings

[0007] The invention is illustrated by way of example and not by way of limitation in the figures of the accompanying drawings, in which the like references indicate similar elements and in which:

[0008] **FIG. 1** is a side cross-sectional view of an array of microelectronic packages in accordance with one embodiment of the present invention;

[0009] **FIG. 2** is a side cross-sectional view of an array of microelectronic packages in accordance with another embodiment of the present invention;

[0010] **FIGs. 3A-3C** are side cross-sectional views showing a process for manufacturing a microelectronic package in accordance with one embodiment of the present invention;

[0011] **FIG. 4** is a side cross sectional view of a known singe-die microelectronic package;

[0012] **FIG. 5** is a side cross sectional view of a known array of microelectronic packages;

[0013] **FIG. 6** is an example system suitable for practicing the present invention in accordance with one embodiment.

[0014] **FIG. 7** illustrates a cross-sectional view of an array of microelectronic packages in accordance with an embodiment of the present invention; and

[0015] **FIG. 8** illustrates a cross-sectional view of an intermediate substrate in accordance with an embodiment of the present invention.

Detailed Description

[0016] **<Beginning of Parent Text >** In the following detailed description, reference is made to the accompanying drawings which form a part hereof wherein like numerals designate like parts throughout, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present invention. Therefore, the following detailed description is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims and their equivalents.

[0017] **FIG. 1** is a side cross sectional view of an array of a microelectronic packages in accordance with an embodiment of the present invention. First microelectronic package 8 comprises a microelectronic die 10 electrically interconnected with a carrier substrate 12. Die 10 is encased in an encapsulation material 14, a common practice in the art. It can be appreciated by one skilled in the art, however, that encapsulation material 14 is provided for a particular purpose, and in other embodiments is not required or provided (*i.e.* optional). Suitable encapsulation materials include, but are not limited to, molded plastic, resins and epoxies.

[0018] Carrier substrate 12 of first microelectronic package 8 has land pads 16 exposed at a die side 9 of carrier substrate 12, outside the periphery of the die 10 and encapsulation material 14. It is understood in the art that the terms "land pads" and "bond pads" are terms for referring to pads, plated through holes, or any other structure that allows for electrical communication between the carrier substrate circuitry and an attached component.

[0019] Intermediate substrate 20 can be mechanically coupled or laminated to the carrier substrate 12, such that it may encompass the periphery of die 10 and encapsulation material 14. Intermediate substrate 20 comprises a variety of dielectric materials, including but not limited to C-stage thermoset polymer resins, epoxies, and the like. In other embodiments that do not include encapsulation material 14, the intermediate substrate 20 can encompass the periphery of die 10, or it may have a cavity that is sized to accommodate the die volume such that it covers die 10.

[0020] Intermediate substrate 20 has a plurality of conductive risers 18 disposed therein. Conductive risers 18 have a first end 13 and a second end 15, and are in relative alignment such that the first end 13 may be in electrical communication with land pads 16 of carrier substrate 12. The second end 15 of conductive risers 18 are also positioned to enable electrical interconnection with bond pads 16' of adjacent second microelectronic package 7. Conductive risers 18 may reduce the size of interconnects 22 needed for electrical interconnection, which may allow for a finer pitch in land pads 16 and bond pads 16'. Conductive risers 18 comprise a variety of conductive materials, including, but not limited to, copper, gold, nickel, and various other metals and metal alloys.

[0021] Second microelectronic package 7 can be positioned adjacent to microelectronic package 8. Microelectronic package 7 may be substantially the same as first microelectronic package 8, and comprises a microelectronic die 10 encased in encapsulation material 14 that is electrically interconnected to a carrier substrate 12. Carrier substrate 12 of second microelectronic package 7 further comprises land pads 16 on the die side 9 and bond pads 16' on the non-die side 11.

[0022] Bond pads 16' are positioned for relative alignment and electrical interconnection with the second end 15 of conductive risers 18 disposed in the intermediate substrate 20 of the first microelectronic package 8. Interconnects 22 electrically interconnect conductive risers 18 with bond pads 16'. Interconnects 22 comprise a conductive material including, but not limited to, leaded solder, lead-free solder, conductive or conductor-filled epoxy, and other conductive substances known to those skilled in the art. Second microelectronic package 7 may also comprise an intermediate substrate 20, having conductive risers 18 disposed therein, in much the same way as discussed above with regard to the intermediate substrate 20 for first microelectronic package 8.

[0023] Third microelectronic package 6 may be positioned adjacent to second microelectronic package 7. Microelectronic package 6 also is substantially the same as first microelectronic package 8, and comprises a microelectronic die 10 encased in encapsulation material 14 that is electrically interconnected to a carrier substrate 12. Carrier substrate 12 of third microelectronic package 6 comprises bond pads 16' on the non-die side 11 of carrier substrate 12. Bond pads 16' of third microelectronic package 6 are positioned for relative alignment and electrical interconnection with the conductive risers 18 of the intermediate substrate 20 of second microelectronic package 7. Interconnects 22 electrically interconnect conductive risers 18 with bond pads 16' of the third microelectronic package 6.

[0024] In addition to the stacked array of three microelectronic packages 8,7,6, as illustrated in **FIG. 1**, other embodiments of stacked arrays in accordance with the present invention may have more or fewer microelectronic packages in the array.

Additionally, the use of the conductive risers 18 may also allow for fine pitch package-to-package interconnection scalability because the height required to clear the adjacent microelectronic package is no longer constrained by interconnects 22, but rather may be dependent on the height and width of the conductive risers 18.

[0025] **FIG. 2** is a side cross sectional view of an array of microelectronic packages in accordance with an embodiment of the present invention. The stacked array comprises multiple microelectronic packages each having one or more stacked microelectronic dice. First microelectronic package 8' has many of the same elements as first microelectronic package 8 as described with respect to FIG. 1. The conductive risers 18' of first microelectronic package 8', however, are slightly elongated in order to accommodate increased package height caused by the additional microelectronic dice 10. The elongated conductive risers 18' then may help to maintain the package to package scalability without increasing the pitch of the land pads 16 or bond pads 16'. Likewise, the conductive risers 18 of second microelectronic package 7' can be adapted to provide a predetermined standoff height for the third microelectronic package 6', again without affecting package to package scalability.

[0026] The gap height 17 between microelectronic packages may be adjusted using different heights of conductive risers for a variety of reasons, including but not limited to accommodate varying microelectronic package thickness. Adjustment to the gap height may also help accommodate additional components such as heat spreaders (not shown), provide a required standoff distance, or increase the pitch of the microelectronic packages without increasing the interconnect 22.

[0027] **FIGs. 3A-3C** are side cross-sectional views showing a process for manufacturing a microelectronic package in accordance with one embodiment of the present invention. **FIG.3A** illustrates an intermediate substrate blank 30 of a predetermined size that has a first side 46 and a second side 48. Adhesive layer 32 can be applied to the second side 48 of intermediate substrate blank 30, which enables the intermediate substrate to couple to the carrier substrate. Adhesive layer 32 may also be applied to the first side 46 of substrate blank 30 to enable the intermediate substrate to be mechanically coupled to the carrier substrate of an adjacent microelectronic package.

[0028] Intermediate substrate blank 30 can be made out of variety of dielectric materials. As previously discussed with regard to intermediate substrate 20 in FIG. 1, one example is the use of a C-stage thermoset polymer resin for intermediate substrate 30 and a B-stage thermoset polymer resin for adhesive layer 32. Use of C-stage and B-stage resins are known in the art and can be done in a variety of ways (further discussed below).

[0029] FIG. 3B is a cross sectional view of the manufacturing process, where the conductive riser 18 may be inserted into an accommodating aperture 35 in substrate blank 30, in accordance with one embodiment. Conductive material 34, having a predetermined thickness, comprises a conductive plating 36 applied to the first end 40 and second end 42 of conductive material 34. Conductive plating 36 enables electrical interconnection with land pads 16 of carrier substrate 12 (shown in FIG. 3C) and bond pads 16' (not shown) of an adjacent microelectronic package. Suitable materials for

conductive plating 36 include, but are not limited to, electrolytic tin plating, lead and lead-free solder.

[0030] Conductive riser 18 can be removed from conductive material 34 using, for example, a punch and die process. Aperture 35 in intermediate substrate blank 30 can be formed by a similar process. As conductive riser 18 is being punched out of conductive material 34, it can be accordingly pressed into aperture 35. Conductive riser 18 and aperture 35 may be created by other techniques, including but not limited to, drilling, augering, laser etching or inserting the conductive material 34 into aperture 35 in a non-solid phase and curing to a solid phase

[0031] The overall thickness of the conductive material 34 and the conductive plating 36 may be the same as or greater than the thickness of the intermediate substrate blank 30, including adhesive layer 32, such that a portion of the conductive plating 36 is flush with or protrudes slightly above the surfaces of the intermediate substrate blank 30 and adhesive layer 32, when inserted in aperture 35. A slight protrusion allows the conductive riser 18 to electrically interconnect with land pads 16 and bond pads 16' (not shown) when the intermediate substrate 30 is secured to a carrier substrate during, for example, a hot press process or during a reflow process. In other embodiments, conductive risers 18 are formed from a conductive material 34 without conductive plating 36. Interconnect (not shown) can also be pre-positioned on the ends of the conductive risers, land pads and/or bond pads such that electrical interconnection is made during a reflow process or the hot press process.

[0032] FIG. 3C is a cross-sectional view of an intermediate substrate fabrication process in accordance with an embodiment of the present invention. Second aperture

38 may be formed in intermediate substrate blank 30, which in turn may complete the formation of the intermediate substrate 31. Second aperture 38 enables intermediate substrate 31 to over lay carrier substrate 12, accommodating the size and shape of the die 10 and, optionally encapsulation material 14. Intermediate substrate 31 may be placed on the die side 44 of carrier substrate 12 of microelectronic package 33, such that the conductive plating 36 of the conductive risers 18 are in electrical communication with corresponding land pads 16. **<End of Parent Text >**

[0033] <Beginning of CIP Material> The intermediate substrate may be mechanically coupled to either carrier substrate, or both, such that it may act as a stiffener to increase the rigidity of a microelectronic package and/or the microelectronic package array. Stiffening the microelectronic package/array may help prevent flex and/or sag in the intermediate substrate, thereby reducing the potential for open circuits leading to flex-induced interconnect failure.

[0034] FIG. 7 illustrates a cross-sectional view of an array of microelectronic packages in accordance with another embodiment of the present invention. First microelectronic package 100 includes a first carrier substrate 112 having a die side 118 and a non-die side 119. A die 110 is coupled to die side 118. Die 110 is covered with encapsulation material 114, though encapsulation material 114 is not required. Land pads 116 are positioned at or near the die side 118 of carrier substrate 112.

[0035] Second microelectronic package 102 includes a second carrier substrate 112' having a die side 118' and a non-die side 119'. A die 110' is coupled to die side 118'. Die 110' is covered with encapsulation material 114', though it can be appreciated

that encapsulation material 114' is not required. Bond pads 117 are positioned at or near the non-die side 119' of carrier substrate 112'.

[0036] Intermediate substrate 120 may be disposed between the die side 118 of the first carrier substrate 112 and the non-die side 119' of the second carrier substrate 112'. Conductive risers 115 may be disposed within intermediate substrate 120. The conductive risers 115 may have a first end 122 and a second end 124. The conductive risers may be positioned such that the first ends may electrically couple with the land pads 116 and the second ends may electrically couple with a corresponding bond pads 117 of the adjacent carrier substrate 112'.

[0037] Intermediate substrate 120 may be mechanically coupled to first carrier substrate 112 and to the second carrier substrate 112, while the conductive risers 115 may be electrically coupled to the land pads 116 of carrier substrate 112 and the bond pads 117. By doing so, the individual packages 100 and 102, as well as the microelectronic package array may become more rigid with respect to each other, such that the array and individual microelectronic packages better resist flexing and warpage. Thus, interconnect, for example solder balls, is not needed in conjunction with the intermediate substrate and conductive risers to control standoff height, as discussed with regard to the embodiments in FIGs. 1 and 2.

[0038] Intermediate substrate 120 can be mechanically coupled to the first and second carrier substrates 112, 112' in a variety of ways, including, but not limited to using B-stage polymers, temperature sensitive adhesives, mechanical fasteners and the like. It can be appreciated that multiple microelectronic packages can continue to be stacked in the array. For brevity, FIG. 7 shows one more microelectronic package 104

mechanically and electrically coupled to an intermediate substrate placed on the die side of microelectronic package 102

[0039] **FIG. 8** illustrates an intermediate substrate 130 in accordance with one embodiment of the present invention. Intermediate substrate 130 may consist of a core 146 having a first side 144 and a second side 145. Core 146 may be made of a C-stage resin, as further described below, or any other material that provides rigidity and does not sag or flex at the maximum processing temperatures. Adhesive layers 148 can be disposed about the first side 144 and second side 145 of the core 146. Adhesive layers 148 may be a B-stage polymer, which when subjected to a suitable process, may mechanically couple the first side 144 of core 146 to the die side of a first carrier substrate and the second side 145 of core 146 to the non-die side of a second carrier substrate (not shown).

[0040] Conductive plating 136 is positioned on the first and second ends of the conductive risers 132. When mechanically coupling the intermediate substrate to adjacent carrier substrates, the conductive risers may be electrically coupled to corresponding land pads and bond pads (not shown) through conductive plating 136.

[0041] The process used to couple the intermediate substrate 130 to a carrier substrate depends on the material used for the adhesive layer 148. In one embodiment, where the core is a C-stage polymer resin and the adhesive layer is a B-stage polymer, a hot press process may be used to mechanically and electrically couple the intermediate substrate to either one or both adjacent carrier substrates. Generally, heat and pressure are applied to the microelectronic packages such that the B-stage polymer and the conductive plating flows and then cures to help ensure an

electrical/mechanical bond between the carrier substrates and the intermediate substrate is created. Where the intermediate substrate is only being mechanically coupled to one carrier substrate, and an interconnect (e.g. solder balls) is being used to electrically interconnect the conductive risers to the adjacent microelectronic package (as discussed with respect to FIGs. 1 and 2), the hot press process may also cause the interconnect to flow and cure thereby creating a electro-mechanical bond.<End of CIP>

[0042] <Parent Text > In one embodiment of a hot press process, where a C-Stage resin for the core of the intermediate substrate and a B-stage resin for adhesive layer are used, a vacuum can be applied such that the pressure within the chamber is less than about 10 kilo Pascals. Heat and pressure may be applied to mechanically couple carrier substrate and intermediate substrate, as well as electrically/mechanically couple land and bond pads to the corresponding conductive risers disposed in the intermediate substrate. Applying a pressure about between 0.5-10 mega Pascals at a temperature about between 150-350 degrees Celsius may provide acceptable lamination of the intermediate substrate to the carrier substrate. Further, this may help ensure electrical coupling between land and bond pads and the conductive risers. The pressure and temperature of the hot press may be varied depending on the properties of the adhesive layer, conductive plating and, if used, interconnect.

[0043] The intermediate substrate material selected may be application dependent, such as to provide a predetermined material stiffness, and/or control the coefficient of thermal expansion (CTE). Thus, other suitable dielectric materials can be used for the intermediate substrate core, including but not limited to various polymer matrix composites. Further, the stiffness of the intermediate substrate can be increased

by adding materials to the core material, such as fiberglass cloth, non woven fabric, composite fibers, and the like.

[0044] **FIG. 6** is an example system suitable for practicing one embodiment of the present invention. A microelectronic package array 92 in accordance with the present invention is coupled to system board 90 through high-speed bus 96. System board 90 may be a carrier substrate, such as a motherboard or other printed circuit boards. As shown, the system board 90 also includes a memory 94 configured to store data, coupled to the system board 90 through high speed bus 96. Memory 94 may include but is not limited to dynamic random access memory (DRAM), synchronous DRAM (SDRAM), and the like. In the embodiment shown, an active cooling mechanism 98 is coupled to the microelectronic package array 92 to help keep the microelectronic package 92 from overheating. Active cooling mechanism may include, but is not limited to fans, blowers, liquid cooling loops and the like.

[0045] Although specific embodiments have been illustrated and described herein for purposes of description of the preferred embodiment, it will be appreciated by those of ordinary skill in the art that a wide variety of alternate and/or equivalent implementations calculated to achieve the same purposes may be substituted for the specific embodiment shown and described without departing from the scope of the present invention. Those with skill in the art will readily appreciate that the present invention may be implemented in a very wide variety of embodiments. This application is intended to cover any adaptations or variations of the embodiments discussed herein. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.